INFORMATION TECHNOLOGY SPECILISATION SCHOOL, INS VALSURA SYLLABUS FOR ENTRANCE EXAM (SAILORS)

This document pertains to the syllabus to be covered by candidates appearing for the entrance exam for Sailors' Course of ITSS. The listed topics need to be covered **broadly** in an analytical manner with focus on the 'whys' behind the facts. The suggested Books of Reference are mostly exhaustive resources and selective reading of the listed topics is considered sufficient. Candidates may not restrict to the suggested Books of Reference till the time the listed topics are well understood from the resource of their choice.

Entrance exam will comprise of a screening test (containing objective type questions) followed by an interview for candidates who attain acceptable grades in the screening test.

Any queries/suggestions are welcome at pdinsvalsura@nic.in.

| 1. | Computer Architecture | | 1.5 | Secor 1.5.1 | ndary Memory Magnetic Storage |
|------------------------|-----------------------------------|-------------------------------|----------------------|--------------------|----------------------------------|
| Book | s/Sites | of Reference:- | | | Optical Storage |
| 1.A | | ured Computer Organisation by | | | Magnetic Tape |
| | ndrew S Tanenbaum | | | | Hard Disk |
| 1.B | | | | | CD/DVD-ROM |
| 1.C | http://www.tomshardware.com | | | | Storage Interfaces |
| | • | | | | IDE, ŠCSI, SATA, SAS |
| Topics to be Covered:- | | | | 1.5.7 | RAID Technologies |
| 1.1 | Histor | y of Computing | | 1.5.8 | Solid State Disks |
| | 1.1.1 | Generation of Computers | 1.6 | IO Te | chnologies |
| | 1.1.2 | Moore's Law | | 1.6.1 | Buses |
| | 1.1.3 | History of x86 Architecture | | | PCI, PCI-Express |
| | and Desktop PCs | | | 1.6.2 | Ports |
| 1.2 | Processors | | | | Parallel, Serial, USB, Fire |
| | 1.2.1 | Internals of CPU | | | wire |
| | | CU, ALU | | 1.6.3 | Display Interfaces |
| | 1.2.2 | • | | | RGB, DVI |
| | | Accumulator, PC, SP etc. | 1.7 | | rn Computer Architecture |
| | 1.2.3 | | | 1.7.1 | |
| | | Fetch, Decode, Data Input | | | MCH, ICH, FSB |
| | | and Execute | | 1.7.2 | |
| | 1.2.4 | | | | Hyper Transport |
| | | Processor and Instruction | | 1.7.3 | Intel Nehalem Architecture |
| | 405 | Level | 4.0 | • | Quick Path Interconnect |
| | | RISC and CISC | 1.8 | | General Knowledge on Latest |
| 1.3 | Memory Hierarchy and Organisation | | PC/Se | erver Ha | |
| | 1.3.1 | Addressing | | | Differences between Server |
| | 1.3.2 | Caching | | and D | esktop Hardware |
| 1.4 | Primary Memory 1.4.1 Volatile | | • | 0 | atin a Creatanna |
| | 1.4.1 | | 2. | <u>Opera</u> | ating Systems |
| | 4 4 0 | SRAM, DRAM | Daale | Dealer of Defenses | |
| | 1.4.2 | Non-volatile | Books of Reference:- | | |
| | | ROM, PROM, EPROM, | 2.A | | rn Operating Systems by |
| | | EEPROM, Flash | Anare | Andrew S Tanenbaum | |

| 2.B | | ating System Concepts by | | | PAN, LAN, CAN, MAN, WAN | |
|------------------------|---|----------------------------------|-------|--------------------------------|--|--|
| | | perschatz, Peter Baer Galvin | 2.2 | Lover | etc. | |
| and G | Greg Ga | gne | 3.3 | 3.2.1 | ng in Networks Need | |
| Tonio | s to bo | Covered | | | | |
| Topics to be Covered:- | | | | | Concept | |
| 2.1 | | ating System Structures | 2.4 | | Advantages | |
| 2.2 | Proce | | 3.4 | | Layer OSI Model of | |
| | | Process Creation | Netwo | orking | | |
| | | Process Termination | | 3.4.1 | , | |
| | 2.2.3 Process States | | 3.6 | | nternet | |
| 2.3 | Threa | | | | IETF and RFCs | |
| | | Thread Model | o = | | TCP/IP Model of Networking | |
| | | Thread Usage | 3.7 | • | cal Layer | |
| 2.4 | | process Communication | | 3.7.1 | Physical Medium | |
| 2.4 | | Scheduling | | Co-axial, Twisted Pair, Fibre, | | |
| 2.5 | | ss Synchronisation | | Wireless | | |
| 2.6 | | ocks (Basics) | | | Modulation and Encoding | |
| 2.7 | | ory Management | | 3.7.3 | , | |
| | | Paging | | | Co-axial, Twisted Pair | |
| | | Virtual Memory | 3.8 | | ink Layer | |
| | 2.7.3 | Swapping | | 3.8.1 | Framing | |
| 2.8 | Input/ | Output Management | | | Bit-level, Byte-level | |
| | 2.8.1 | Programmed Input/Output | | | Bit-stuffing, Byte-stuffing | |
| | 2.8.2 | Direct Memory Access | | 3.8.2 | Error Detection/Correction | |
| | 2.8.3 | | | | Framing in Ethernet | |
| | | Interrupt Handlers | 3.9 | MAC S | Sub-layer | |
| | 2.8.4 | Device Drivers | | 3.9.1 | Multiple Access Techniques | |
| 2.9 | File S | ystem | | | CSMA-CD, CSMA-CA | |
| | 2.9.1 | File Naming, Structure, | | | Token Ring | |
| | Types | s, Access and Attributes | | 3.9.3 | ALOHA | |
| | | File Operations | | 3.9.4 | MAC in Ethernet | |
| | | • | 3.10 | Netwo | ork Layer | |
| | | File System Layout | | | Hierarchical Addressing | |
| | 2.9.5 | Disk Space Management | | | Circuit Switching and Packet | |
| | | 2 1 | | Transf | | |
| 3. | Comp | outer Networking | | | Types of Routing | |
| - | <u></u> | <u> </u> | | 0 | Fixed, Source, Dynamic | |
| Books of Reference:- | | | | 3.10.4 | Basics of Routing Protocols | |
| 3.A | | outer Networks by Larry L | | 0 | Distance Vector, Link State | |
| | • | Bruce S Davie | | 3 10 5 | Internet Protocol v4 | |
| 3.B | | outer Networks by Andrew S | | | Subnet and Gateway | |
| | nbaum | rator Networks by Amarew C | | | Classless Inter-domain | |
| Tarici | ibaaiii | | | Routir | | |
| Tonic | e to be | Covered:- | | | DHCP, ARP and RARP | |
| 3.1 | | to be Covered:- | | | port Layer | |
| J. I | Definition of Computer Networking 3.1.1 Bandwidth and Latency | | 3.11 | | Multiplexing | |
| 2.0 | | • | | | | |
| 3.2 | 3.4.1 | ification of Computer Network | | | Reliability using | |
| | 3.4.1 | Topology Star Moch Troo Rus Ping | | | wledgements | |
| | | Star, Mesh, Tree, Bus, Ring | | | S Sliding Window Protocol TCP and UDP | |
| | 2 4 2 | etc. | | 3.11.4 | | |
| | 3.4.2 | Type/Size | | | Concept of Ports | |

- 3.11.5 Connections in TCP
- 3.12 Application Layer
 - 3.12.1 DNS
 - 3.12.2 Electronic Mail
 - 3.12.3 World Wide Web
 - 3.12.4 FTP

4. Database Concepts

Books of Reference:-

4A. Database System Concepts by Abraham Silberschatz, Henry F Korth and S Sudarshan

Topics to be Covered:-

- 4.1 Database Systems
 - 4.1.1 Purpose
 - 4.1.2 Data Abstraction
- 4.2 Relational Databases
 - 4.2.1 Structure
 - 4.2.2 Relational Algebra

5. Digital Logic

Books of Reference:-

5A. Digital Logic and Computer Design by M Morris Mano

Topics to be Covered:-

- 5.1 Binary Systems
 - 5.1.1 Digital Computers and Systems
 - 5.1.2 Binary Numbers
 - 5.1.3 Number Base Conversion Binary, Octal, Decimal, Hexadecimal
 - 5.1.4 Complements
 - 5.1.5 Binary Codes
 Binary Coded Decimal
 - 5.1.6 Binary Storage
 - 5.1.7 Binary Logic
- 5.2 Boolean Algebra
 - 5.2.1 Basic Theorems and
 - **Properties**
 - 5.2.2 Boolean Functions
 - 5.2.3 Logical Operations
- 5.3 Digital Logical Gates
- 5.4 Basics of Probability and Statistics

6. <u>Linux and Windows</u>

General References

Topics to be Covered:-

- 6.1 Linux Operating System
 - 6.1.1 Installation (of any latest flavour)
 - 6.1.2 Installation of Applications
 - 6.1.3 Exploitation of Command Line Interface
- 6.2 Windows Operating System
 - 9.2.1 Installation (of any version)
 - 9.2.2 Installation of Applications